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(54) Title: METHOD FOR HIGH TEMPERATURE ETCHING OF PATTERNED LAYERS USING AN ORGANIC MASK STACK			
<p>A B C D E F G</p>			
(57) Abstract			
<p>The present disclosure pertains to a method of patterning a semiconductor device feature which provides for the easy removal of any residual masking layer which remains after completion of a pattern etching process. The method provides for a multi-layered masking structure which includes a layer of high-temperature organic-based masking material overlaid by either a layer of a high-temperature inorganic masking material which can be patterned to provide an inorganic hard mask, or by a layer of high-temperature imageable organic masking material which can be patterned to provide an organic hard mask. The hard masking material is used to transfer a pattern to the high-temperature organic-based masking material, and then the hard masking material is removed. The high-temperature organic-based masking material is used to transfer the pattern to an underlying semiconductor device feature.</p>			

METHOD FOR HIGH TEMPERATURE ETCHING OF
PATTERNED LAYERS USING AN ORGANIC MASK STACK

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains to a method for patterned etching of materials such as copper, platinum, iridium, ruthenium, tungsten, and barium strontium titanate, which generally requires higher temperature stability of the stack of masking materials used during the patterned etching. In addition to high temperature functionality, the stack of masking materials is designed to minimize the amount of masking material residue and sidewall deposits remaining on feature surfaces after etching.

2. Brief Description of the Background Art

In the field of semiconductor device fabrication, particularly with the continuing trend toward smaller device feature sizes, the etch processes which are used to construct conductive features such as metal interconnects and contacts have become particularly critical. The new devices, having feature sizes in the range of about 0.25 μm and smaller, place an emphasis on both the precise profile achievable during pattern etching and on the avoidance of any residue remaining after etch which causes problems during subsequent processing or problems in long term device function.

We previously worked to develop a plasma etching system which reduces and avoids the formation of residue on the surface of a copper layer during pattern etching. The etching systems useful in etching of the conductive material are described in copending application Serial Nos. 08/891,410, filed July 9, 1997, and 08/911,878, filed August 13, 1997 (Docket No. AM-2181), both of which are hereby incorporated by reference and both of which are assigned to the assignee of the present application.

We have simultaneously been working to develop an etching process which permits the development of patterning masks which can transfer a desired pattern to adjacent layers in a manner which reduces or avoids the formation of mask residue on the

etched structure.

Figures 1A - 1E show a schematic cross-sectional view of a typical plasma etch stack useful at temperatures in excess of about 150 °C as it progresses through a series of steps including the etching of a feature layer. This etch stack is of the kind known and used prior to the present invention. Figure 1A shows a complete etch stack, including: Substrate 102, which is typically a dielectric layer overlying a semiconductor substrate (such as a silicon wafer substrate) or which may be the semiconductor material itself, depending on the location on a given device surface. Barrier layer 104, which prevents the diffusion and/or migration of material between conductive layer 106 and substrate 102; conductive layer 106, which is typically aluminum or copper, but might be tungsten, platinum, iridium or rubidium, for example. Anti-reflective-coating (ARC) layer 108, which is typically a metal-containing compound and which enables better imaging of an overlying patterning layer. The ARC layer also frequently serves as a barrier layer to prevent diffusion/migration between conductive layer 106 and overlying pattern masking layer 110. Pattern masking layer 110, which is typically a layer of silicon dioxide or similar inorganic material which can withstand the high temperatures encountered during etching of conductive layer 106, and which can be patterned and used as a mask during such etching. And, photoresist layer 112 which is typically an organic-based material which is stable at low temperatures and which is used to pattern masking layer 100, which is stable at higher temperatures. In Figure 1A, photoresist layer 112 has already been patterned to provide the feature shape desired to be transferred to pattern masking layer 100.

Figure 1B shows the stack described in Figure 1A, where the pattern in photoresist layer 112 has been transferred to pattern masking layer 110, using a standard plasma etching technique. When masking layer 110 comprises a silicon-containing material, such as silicon dioxide, the etch plasma typically comprises a fluorine-generating species. Preferably the plasma selectivity is for the silicon dioxide over the photoresist material.

Figure 1C shows the next step in the process of etching conductive layer 106,

where the photoresist layer 112 has been stripped from the surface of pattern masking layer 110. This stripping procedure may be a wet chemical removal or may be a plasma etch which is selective for the photoresist layer 112 over the pattern masking layer 110. Stripping of photoresist layer 112 is carried out for two reasons. The organic-based photoresist materials typically used for layer 112 would melt or become distorted in shape at the temperatures commonly reached during the etching of conductive layer 106. This could lead to distortion of the pattern which is transferred to conductive layer 106. In addition, polymeric species generated due to the exposure of the surface of photoresist layer 112 to the etchant plasma tend to contaminate adjacent surfaces during the etching of conductive layer 106, thereby decreasing the etch rate of conductive layer 106. The procedure of using a photoresist material to pattern an underlying silicon oxide patterning layer is described in U.S. Patent No. 5,067,002 to Zdebel et al., issued November 19, 1991. Zdebel et al. mention the need to remove the photoresist material prior to etching of underlying layers, to avoid contamination of underlying surfaces with the photoresist material during etching of such underlying layers. David Keller describes the use of an ozone plasma for the purpose of dry etch removal of a photoresist mask from the surface of an oxide hard mask in U.S. Patent No. 5,346,586, issued September 13, 1994. Mr. Keller also mentions that it is easier to etch selectively to a gate oxide when there is no photoresist present during a polysilicon gate oxide etch step.

Figure 1D shows the next step in the etching process, where the desired pattern has been transferred through ARC layer 108, conductive layer 106, and barrier layer 104. Typically all of these layers are metal comprising layers, and a halogen containing plasma can be used to etch the pattern through all three layers. At this point, the problem is the removal of the residual silicon dioxide hard masking material and the removal of residue deposits of the silicon dioxide masking material from adjacent surfaces. The residual hard masking material is present as residual masking layer 110, and the residue deposits as 114 on the surface of the patterned conductive layer 106 and the surface of substrate 102.

In the case of the deposit 114 on the surface of patterned conductive layer 106,

deposit 114 can trap residual chemical etch reactants under deposit 114 and against the surface of patterned conductive layer 106, leading to subsequent corrosion of conductive layer 106. That corrosion is shown on Figure 1D as 116.

In addition, when substrate 102 is a low dielectric constant material, for purposes of increasing the gate speed of a field effect transistor, residual masking layer 110 which remains after pattern etching through layers 108, 106, and 104 (as shown in Figure 1D) can reduce device performance. This makes it important to remove any residual masking layer 110 from the surface of ARC layer 108.

Further, when a dielectric layer 118 is applied over the surface of the patterned conductive layer 106, as shown in Figure 1E, if residual masking layer 110 is not removed, a non-planar surface 120 is produced. A non-planar surface creates a number of problems in construction of a multi-conductive-layered device, where additional patterned conductive layers (not shown) are constructed over the surface 120 of dielectric layer 118.

With the above considerations in mind, we wanted to develop a patterning system, including a multi-layered structure and a method for its use which would provide for the easy removal of residual masking layer material after completion of the patterning process.

SUMMARY OF THE INVENTION

The present disclosure pertains to a method of patterning a semiconductor device feature which provides for the easy removal of any residual masking layer which remains after completion of a pattern etching process. The method provides for a multi-layered masking structure which includes a layer of high-temperature organic-based masking material overlaid by either a layer of a high-temperature inorganic masking material which can be patterned to provide an inorganic hard mask, or by a layer of high-temperature imageable organic masking material which can be patterned to provide an organic hard mask. The hard masking material is used to transfer a pattern to the high-temperature organic-based masking material, and then the hard masking material is

removed. The high-temperature organic-based masking material is used to transfer the pattern to an underlying semiconductor device feature. The high-temperature organic-based masking material can be removed from the surface of the patterned semiconductor device feature in a manner which reduces or avoids contamination of the patterned feature surface.

In accordance with the present invention, we have developed two patterning systems which enable the patterning of underlying layers at relatively high temperatures, ranging between about 150 °C and about 500 °C, while providing easy removal of any residual masking layer remaining after the patterning process.

The first patterning system uses a multi-layered masking structure which includes a layer of high-temperature organic-based masking material overlaid by a layer of a high-temperature inorganic masking material, which is further overlaid by a layer of a patterning photoresist.

The patterning method is as follows.

a) The layer of photoresist material is imaged and developed into a pattern using techniques known in the art, to produce a patterned mask which can be used to transfer the desired pattern throughout the multi-layered masking structure and eventually through at least one device feature layer as well.

b) The patterned photoresist is used to transfer the pattern through

i) a layer of high-temperature inorganic masking material; and

ii) a layer of high-temperature organic-based masking material.

Preferably the pattern transfer through the layer of high-temperature organic-based masking material is via an anisotropic plasma etch technique so that this material is not undercut by the pattern transfer process.

c) Residual photoresist which remains after pattern transfer is then removed from the multilayered structure by plasma etch, using the high-temperature inorganic masking layer as an etch stop. The photoresist removal is accomplished using an anisotropic etch process which typically comprises an oxygen-based plasma etch. The anisotropic stripping of the photoresist prevents or at least substantially reduces any etching of the

high-temperature organic-based masking material during photoresist removal.

d) Optionally, the layer of high temperature inorganic masking material may be removed at this time using a plasma etch technique or a wet etch technique designed to minimize any etching of the organic-based masking material. Preferably, the high temperature inorganic masking material is of a thickness such that it will be automatically removed during etching of a feature layer (step e).

(e) The pattern is then transferred from the high-temperature organic-based masking layer through at least one feature layer underlying the high-temperature organic-based masking material.

f) Any high-temperature organic-based masking material remaining after feature layer patterning is then easily removed using a plasma etch technique. When the etched feature layer would be corroded or oxidized by an oxygen-based plasma, a hydrogen-based plasma etch technique is recommended. The removal of organic-based masking material may be by a wet stripping technique using a solvent known in the art to be advantageous in the passivation of the surface of the patterned feature layer.

Since there is no residual photoresist material remaining from step a) present during etching of the feature layer, there is no layer which is likely to melt or distort in shape during transfer of the pattern from the high-temperature organic-based masking material to an underlying device feature layer.

Since the high-temperature organic-based masking layer is easily removed, there need be no residual masking layer present in the device structure to affect device performance or to cause planarization difficulties. Preferably, the high-temperature organic-based masking layer is formed from α -C and α -FC films deposited using CVD techniques. Examples of starting materials used to form such films include CH_4 , C_2H_2 , CF_4 , C_2F_6 , C_4F_8 , NF_3 , and combinations thereof; there are, of course, numbers of other carbon-containing precursor materials which can also be used.

The second patterning system is different from the first patterning system in that

it uses a high-temperature pattern-imaging layer rather than a more standard photoresist imaging layer. The high-temperature pattern-imaging layer is stable at temperatures ranging from about 150 °C to about 500 °C, compared with photoresist materials which are generally stable at about 150 °C or lower. Preferably the high-temperature pattern-imaging layer is a plasma-polymerized material, such as plasma polymerized methyl silane (PPMS), which may be imaged by deep UV and which is plasma-developable.

The patterning method is as follows.

- a) A layer of high-temperature imageable material is imaged and developed into a pattern using techniques known in the art, to produce a patterned mask which can be used to transfer the desired pattern through the high-temperature organic-based masking material and eventually through at least one device feature layer.
- b) After patterning of the high-temperature imageable material, the pattern is transferred through the underlying layer of high-temperature organic-based masking material. Preferably the pattern is transferred via an anisotropic etch technique, whereby the high-temperature organic-based masking material is not undercut by the pattern transfer step.
- c) The pattern is then transferred from the multi-layered structure formed in steps a) and b) through at least one feature layer underlying the high-temperature organic-based masking material. Preferably the pattern is transferred using an anisotropic etching technique so that any high-temperature imageable material which might remain from step b) is removed during this pattern transfer step. In addition, the use of an anisotropic etching technique reduces or avoids the possibility of undercutting the high-temperature organic-based material layer during the pattern transfer to the underlying device feature layer.
- d) Any residual high-temperature organic-based masking material which remains after pattern transfer is then easily removed using a plasma etch technique. When the etched feature layer would be corroded or oxidized by an oxygen-based plasma, a hydrogen-based plasma etch technique is recommended.

Since there is no low temperature residual photoresist material used during this process, there is no layer which is likely to melt or distort in shape during transfer of the pattern from the high-temperature organic masking material to an underlying device feature layer.

The high-temperature imageable material is preferably of the kind which can be produced using a silane-based starting material or TEOS-based (tetra-ethyl-ortho-silicate - based) chemistry, although one skilled in the art may select from other materials known in the art.

The high-temperature organic-based masking material is preferably chosen from materials which can be easily removed by plasma etch techniques or by using a solvent known in the art to be advantageous in the passivation of the surface of the patterned feature layer. Examples of such materials are provided above with reference to the first patterning system.

When the at least one device feature layer which is to be patterned includes a copper layer, that copper layer is preferably pattern etched using either an enhanced physical bombardment technique or a plasma etching technique which generates sufficient hydrogen to protect the copper surface during patterning.

The most economical method of performing the etch techniques described above utilizes a combination of different plasmas wherein the different etchant gases used to create each plasma are sufficiently compatible that all of the etching steps can be carried out in individual (separate) steps in the same etch chamber, if desired. One skilled in the art can select from the various known plasma etchants to obtain the best economies of function which will provide etched features meeting dimensional and surface stability requirements.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A through 1E show a schematic of the cross-sectional view of a prior art multilayered structure useful in plasma etching (a plasma etch stack), as the etch stack progresses through a series of process steps. This etch stack is generally used for etching

of a device feature conductive material layer.

Figure 2A shows a schematic of the cross-sectional view of a first preferred embodiment plasma etch stack of the present invention. Figures 2B through 2G show the changes in the etch stack as it progresses through the method steps of the present invention.

Figure 3A shows a schematic of the cross-sectional view of a second preferred embodiment plasma etch stack of the present invention. Figures 3B through 3G show the changes in the etch stack as it progresses through the method steps of the present invention.

Figure 4 is a schematic of a process chamber and auxiliary apparatus of the kind which can be used to carry out the plasma etching steps described herein.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In accordance with the present invention, we have developed two patterning systems which enable the patterning of underlying layers while providing for the easy removal of masking layers used to accomplish the patterning.

I. DEFINITIONS

As a preface to the detailed description, it should be noted that, as used in this specification and the appended claims, the singular forms "a", "an", and "the" include plural referents, unless the context clearly dictates otherwise. Thus, for example, the term "a semiconductor" includes a variety of different materials which are known to have the behavioral characteristics of a semiconductor, reference to a "plasma" includes a gas or gas reactants activated by an RF glow discharge, reference to "a conductive material" includes aluminum, aluminum alloys, copper, copper alloys, platinum, platinum alloys,

iridium, iridium alloys, rubidium, ruthenium, ruthenium oxide, combinations thereof, and other conductive materials which would be suitable in the application described.

Specific terminology of particular importance to the description of the present invention is defined below.

The term " α -C" refers to high temperature amorphous carbon-comprising materials which are typically produced by CVD in a plasma chamber.

The term " α -FC" refers to high temperature fluorocarbon materials which are typically produced by CVD in a plasma chamber.

The term "aluminum" includes alloys of aluminum of the kind typically used in the semiconductor industry. Such alloys include aluminum-copper alloys, and aluminum-copper-silicon alloys, for example. Typically such alloys of aluminum comprise about 0.5 % copper.

The term "anisotropic etching" refers to etching which does not proceed in all directions at the same rate. If etching proceeds exclusively in one direction (e.g. only vertically), the etching process is said to be completely anisotropic.

The term "bias power" refers to the power used to control ion bombardment energy and the directionality of ions toward a substrate.

The term "copper" refers to copper and alloys thereof, wherein the copper content of the alloy is at least 80 atomic % copper. The alloy may comprise more than two elemental components.

The term "feature" refers to metal lines and openings on a substrate, and other structures used to form a semiconductor device.

The term "hydrogen-based plasma" refers to a plasma having a sufficiently high hydrogen content to reduce the corrosion of the exterior surfaces of etched features by incident reactive species which are present due to etching of adjacent surfaces. A preferred example of a hydrogen-based plasma is described in co-pending application Serial No. 08/911,878, filed August 13, 1997. Typically, a hydrogen-based plasma, in addition to a source of hydrogen, will include other additives comprising fluorine, or chlorine, or oxygen, or nitrogen, or carbon, or a combination thereof, by way of example

and not by way of limitation.

The term "ion bombardment" refers to physical bombardment by ions (and other excited species of atoms which are present with the ions) to remove atoms from a surface, where physical momentum transfer is used to achieve the atom removal.

The term "isotropic etching" refers to an etching process where etching can proceed in all directions at the same rate.

The term "oxygen-based plasma" refers to a plasma which is rich in oxygen content either in neutral or charged form. The plasma may include additives comprising nitrogen, or hydrogen, or chlorine, or fluorine, or carbon, by way of example and not by way of limitation. Additives such as CF_4 , CH_4 and NH_3 are commonly used.

The term "plasma" refers to a partially ionized gas containing an equal number of positive and negative charges, as well as some other number of non-ionized gas particles.

The term "plasma-polymerized methysilane" refers to a new deep UV resist material which is deposited from a low power RF plasma discharge in methysilane at room temperature. This material possesses an amorphous organosilicon hydride network structure. While initially opaque in the deep UV (i.e. 248 nm), a typical 0.25 micron thick film undergoes efficient photooxidation with bleaching to form glass-like siloxane network material.

The term "source power" refers to the power used to generate ions and neutrals whether directly in an etching chamber or remotely as in the case of a microwave plasma generator.

The term "substrate" includes semiconductor materials, glass, ceramics, polymeric materials, and other materials of use in the semiconductor industry.

II. AN APPARATUS FOR PRACTICING THE INVENTION

The preferred embodiment etch processes described herein were carried out in a Centura® Integrated Processing System available from Applied Materials, Inc. of Santa Clara, California. The system is shown and described in United States Patent No. 5,186,718, the disclosure of which is hereby incorporated by reference. This equipment

included a Decoupled Plasma Source (DPS) of the kind described by Yan Ye et al. at the Proceedings of the Eleventh International Symposium of Plasma Processing, May 7, 1996 and as published in the Electrochemical Society Proceedings, Volume 96-12, pp. 222 - 233 (1996). The plasma processing chamber enables the processing of an 8 inch (200 mm) diameter silicon wafer.

A schematic of the processing chamber is shown in Figure 4 which shows an etching process chamber 410, which is constructed to include at least one inductive coil antenna segment 412 positioned exterior to the etch process chamber 410 and connected to a radio frequency (RF) power generator 418. Interior to the process chamber is a substrate 414 support pedestal 416 which is connected to an RF frequency power generator 422 through an impedance matching network 424, and a conductive chamber wall 430 which serves as the electrical ground 434 for the offset bias which accumulates on the substrate 414 as a result of the RF power applied to the substrate support pedestal 416.

The semiconductor substrate 414 is placed on the support pedestal 416 and gaseous components are fed into the process chamber through entry ports 426. A plasma is ignited in process chamber 410 using techniques well known in the industry. Pressure interior to the etch process chamber 410 is controlled using a vacuum pump (not shown) and a throttle valve 427 connected to a process chamber gas exit line 428. The temperature on the surface of the etch chamber walls is controlled using liquid-containing conduits (not shown) which are located in the walls of the etch chamber 410. For experimental purposes, it was desired to maintain the substrate temperature above about 150 °C and below about 350 °C, and this was accomplished using a resistivity heater applied to the substrate support pedestal. The surface of the etching chamber 410 walls was maintained at about 80 °C using the cooling conduits previously described. In the case of a production process, preferably, the substrate support platen provides for backside heating or cooling of the substrate.

III. THE FIRST PREFERRED EMBODIMENT ETCH STACK

AND ITS METHOD OF USE

Figures 2A - 2G illustrate the first preferred embodiment etch stack of the present invention as it progresses through the method steps of the present invention. Figure 2 A shows the complete etch stack, including: Substrate 212, which was a dielectric layer of silicon dioxide approximately 1,000 Å thick overlying a silicon wafer surface (not shown). A barrier layer 214, of tantalum nitride approximately 500 Å thick was deposited over substrate 212. A layer 216 of copper approximately 8,000 Å thick was deposited over barrier layer 214. A layer 218 of tantalum nitride about 500 Å thick, which served as a barrier layer, was deposited over copper layer 216.

A layer 220 of a high-temperature organic-based pattern masking material comprising α -FC was deposited over tantalum nitride layer 218 using a high density plasma CVD technique, to produce a layer approximately 8,000 Å thick. A silicon dioxide pattern masking layer 222, approximately 1,000 Å thick, which served as a high-temperature inorganic masking material was applied over the high-temperature α -FC layer 220. And, finally, a photoresist imaging layer 224, of I - line stepper material (any of these materials which are commonly used in the art are acceptable) approximately 10,000 Å thick was applied over the surface of high-temperature inorganic masking material layer 222.

In Figure 2A, I - line photoresist imaging layer 224 has already been patterned to provide the feature shape desired to be transferred to the silicon dioxide pattern masking layer 222 and high-temperature organic-based masking layer 220. Preferably, the thickness of photoresist imaging layer 224 is designed so that it is nearly totally consumed during transfer of the pattern through the high-temperature inorganic masking layer 222 and high-temperature organic-based masking layer 224.

Figure 2B shows the plasma etching stack described in Figure 2A, where the pattern in photoresist imaging layer 224 has been transferred through the high temperature silicon dioxide inorganic pattern masking layer 222 and through the α -FC-comprising layer 220, to reach the upper surface of tantalum nitride barrier layer 218.

This pattern transfer was accomplished using an oxygen-based plasma in the Centura® Integrated Processing System previously described. During the etching of silicon dioxide layer 222, the plasma feed gas to the process chamber was about 100 sccm of argon and 30 sccm of CHF₃. The substrate temperature during etching was about 20 °C, with the process chamber walls at about 80 °C. The process chamber pressure during etching was about 10 mT. The source power to the plasma inducing coil was about 1800 W @ 2 MHz and the bias power to the substrate support platen was about 300 W @ 13.56 MHz. A plasma was ignited using techniques standard in the art, and the time period required for pattern transfer through silicon dioxide layer 222 was approximately 15 seconds. During the etching of α-FC layer 220, the plasma feed gas to the process chamber was 100 sccm of O₂, and 10 sccm of N₂. The substrate temperature during etching was about 20 °C, with the process chamber walls at about 80 °C. The process chamber pressure during etching was about 10 mT. The source power to the plasma inducing coil was about 1000 W @ 2 MHz and the bias power to the substrate support platen was about 250 W @ 13.56 MHz. The time period required for pattern transfer through α-FC layer 220 was approximately 80 seconds.

Figure 2C shows the plasma etching stack described in Figure 2B, after removal of residual photoresist imaging layer 224. Residual photoresist imaging layer 224 was removed using an O₂ / N₂ plasma. The plasma feed gas to the process chamber was 100 sccm of O₂ and 10 sccm of N₂. The substrate temperature during etching was about 20 °C, with the process chamber walls at about 80 °C. The process chamber pressure during etching was about 10 mT. The source power to the plasma inducing coil was about 1,000 W @ 2 MHz and the bias power to the substrate support platen was about 250 W @ 13.56 MHz. A plasma was ignited using techniques standard in the art, and the time period required for the removal of the residual photoresist material was about 20 seconds. The underlying layer 222 of silicon dioxide was used as an etch stop over high-temperature organic-based layer 220, while tantalum nitride barrier layer 218 was used as the etch stop protecting copper layer 216. The plasma and process conditions described above provided anisotropic stripping of photoresist imaging layer 224, so that

high-temperature α -FC masking layer 220 would not be undercut during the removal of residual photoresist imaging layer 224. Generally, any oxidizing plasma can be used to remove most photoresist materials.

Figure 2D shows an optional step in which the layer 222 of silicon dioxide may be removed. However, for most applications, such as this application where feature layer 216 comprises a metal (copper), if the thickness of silicon dioxide layer 222 is properly designed, this layer will be automatically removed during the patterning of feature layer 216.

Figure 2E shows the plasma etching stack after transfer of the pattern through tantalum nitride barrier layer 218, copper layer 216, and tantalum nitride barrier layer 214 to the upper surface of silicon dioxide dielectric layer 212. This etching of the conductive copper layer 216 and accompanying barrier layers 218 and 214 was accomplished using a feed gas to the process chamber of 70 sccm of HCl, 50 sccm of N₂, and 5 sccm of BCl₃. The substrate temperature during etching was about 250 °C, with the process chamber walls at about 80 °C. The process chamber pressure during etching was about 20 mT. The source power to the plasma inducing coil was about 1,500 W @ 2 MHz and the bias power to the substrate support platen was about 600 W @ 13.56 MHz. The end point of etch through tantalum nitride barrier layer 214 was measured by optical monitoring using a sensor measuring at a wavelength of about 3,590 Å. The time period required for pattern transfer through the tantalum nitride barrier layer 218, copper layer 216, and tantalum nitride barrier layer 214 was about 150 seconds. A hydrogen-based etch chemistry was used during patterning of the copper feature layer 216 to avoid corrosion of the copper. Use of a conventional oxygen and fluorine based chemistry may induce oxidation/corrosion.

Depending on the relative thicknesses of layers α -FC layer 220, tantalum nitride 218, copper layer 216, and tantalum nitride layer 214 and the etching conditions used, there should be enough of the α -FC layer 220 remaining at the end of the etch process to provide CD (critical dimension) control. Therefore, a separate process is needed to remove the remaining portion of this α -FC layer. The process for stripping the α -FC

layer may be carried out in the feature patterning etch chamber or in a downstream plasma chamber.

Figure 2F shows the patterned feature layer 216 with accompanying barrier layers 214 and 218, after removal of the remaining portion of the α -FC layer 220. Preferably the α -FC layer 220 is removed via anisotropic stripping using a hydrogen based chemistry of the kind described above or a wet stripping process using a solvent which assists in the passivation of the etched copper feature surface. In the present instance, an anisotropic dry stripping technique was used, wherein the feed gas to the process chamber was 100 sccm of H_2 . The substrate temperature during etching was about 45 °C, with the process chamber walls at about 80 °C. The process chamber pressure during etching was about 10 mT. The source power to the plasma inducing coil was about 1,000 W @ 2 MHz and the bias power to the substrate support platen was about 200 W @ 13.56 MHz. The time period required for stripping of the remaining portion of the α -FC layer 220 was about 120 seconds.

Figure 2G shows the application of a planarization layer 230 of a low dielectric constant material such as an α -C or an α -FC over patterned tantalum nitride layer 218, copper layer 216, tantalum nitride layer 214, and silicon dioxide substrate 212. The planarization layer exhibited a truly planar surface, rather than the non-planar surface 120 observed for the prior art planarization layer illustrated in Figure 1E. Preferably the α -C or an α -FC is applied using a vapor deposition technique known in the art, although spin-on techniques, for example, are also acceptable.

One skilled in the art will recognize that high-temperature inorganic masking materials other than silicon oxide can be used as the capping layer overlying the high-temperature organic-comprising masking material. In addition, one skilled in the art will recognize that high-temperature organic-based masking materials other than α -FC, such as α -C, polyimide, parylene, and teflon, for example, can be used. Anti-reflective/barrier layer materials other than tantalum nitride, such as silicon oxynitride, tantalum, titanium nitride, tungsten titanate, and tungsten nitride may also be used. And finally, the method is not limited to the etching of device features which utilize copper as the conductive

material. Other conductive materials such as tungsten, platinum, silver, gold, iridium, and ruthenium, for example can be used as well.

IV. THE SECOND PREFERRED EMBODIMENT ETCH STACK AND ITS METHOD OF USE

Figures 3A - 3G illustrate the second preferred embodiment etch stack of the present invention and its progression through the method steps of the present invention. Figure 3A shows the complete etch stack, including: Substrate 312, which was a dielectric layer of silicon dioxide approximately 10,000 Å thick overlying a silicon wafer surface (not shown). A barrier layer 314, of tantalum nitride approximately 500 Å thick was deposited over substrate 312. A layer 316 of copper approximately 8,000 Å thick was deposited over barrier layer 314. A layer 218 of tantalum nitride about 500 Å thick was deposited over copper layer 216. A layer 220 of a high-temperature organic-based pattern masking material comprising α -FC was deposited over titanium nitride layer 218 using a high density plasma CVD technique, to produce a layer approximately 8,000 Å thick. And, finally, a layer 322 of plasma polymerized methylsilane (PPMS) was deposited from a low power RF plasma discharge in methylsilane at room temperature, to produce a layer approximately 1,000 Å thick.

Subsequently, the PPMS layer was exposed to deep UV with bleaching to produce a glass-like siloxane pattern 324 within PPMS layer 322, as shown in Figure 3B.

Figure 3C illustrates the pattern development of the PPMS high temperature imaging layer 324, which was developed using chlorine plasma etching by techniques known in the art (as described by T.W. Weidman et al., *Journal of Photopolymer Science and Technology*, Volume 8, Number 4, 679 - 686 (1995)).

Subsequently, as shown in Figure 3D, the underlying α -FC layer 320 was etched using an oxygen-based plasma in the manner described above with reference to Figure 2B, where α -FC layer 220 was patterned. The time period required for pattern transfer through α -FC layer 320 was approximately 80 seconds. The oxygen-based plasma

chemistry was chosen so that the patterned silicon dioxide 324 formed from the high-temperature imageable material (PPMS) layer 322 and tantalum nitride barrier layer 318 would not be attacked during etching of α -FC layer 320. The oxygen-based etch conditions referenced above provided anisotropic etch conditions so that undercutting of the α -FC layer 320 during pattern development was avoided.

Figure 3E shows the transfer of the pattern through tantalum nitride barrier layer 318, copper layer 316, and tantalum nitride barrier layer 314 to the upper surface of silicon dioxide dielectric layer 312. This etching of the conductive copper layer 316 and accompanying barrier layers 318 and 314 was accomplished using the method described with reference to Figure 2E.

Depending on the relative thicknesses of layers α -FC layer 320, tantalum nitride 318, copper layer 316, and tantalum nitride layer 314 and the etching conditions used, there should be enough of the α -FC layer 320 remaining at the end of the etch process to provide CD (critical dimension) control. Therefore, a separate process is needed to remove the remaining portion of this α -FC layer. The process for stripping the α -FC layer may be carried out in the feature patterning etch chamber or in a downstream plasma chamber.

Figure 3F shows the patterned feature layer 316 with accompanying barrier layers 318 and 314, after removal of the remaining portion of the α -FC layer 320. Preferably the α -FC layer 320 is removed via anisotropic stripping using a hydrogen based chemistry of the kind described above or a wet stripping process using a solvent which assists in the passivation of the etched copper feature surface. In the present instance, an anisotropic dry stripping technique, as described with reference to Figure 2F was used.

Figure 3G shows the application of a planarization layer 328 of a low dielectric constant material such as an α -C or an α -FC over the patterned tantalum nitride layer 318, copper layer 316, tantalum nitride layer 314, and silicon dioxide substrate 312. The planarization layer exhibited a truly planar surface, rather than the non-planar surface 120 observed for the prior art planarization layer illustrated in Figure 1E. Preferably the α -C or an α -FC is applied using a vapor deposition technique known in the art, although

spin-on techniques, for example, are also acceptable.

One skilled in the art will recognize that high-temperature imageable masking materials other than PMMS can be used as the layer for pattern transfer to the high-temperature organic-comprising masking material. In addition, one skilled in the art will recognize that other high-temperature organic-based masking materials, ARC materials, barrier layer materials, and conductive materials, such as those previously listed (and not by way of limitation) can be used.

It is important to mention that when copper is used as the conductive material, the etching methods disclosed in U.S. Application Serial No. 08/891,410, and 08/911,878, referenced above, are recommended for use in combination with the methods of the invention described herein.

In particular, Application Serial No. 08/891,410 discloses that copper can be pattern etched at acceptable rates and with selectivity over adjacent materials using an etch process which utilizes a solely physical basis such as ion bombardment, without the need for a chemically based etch component.

A first preferred enhanced physical bombardment technique requires an increase in ion density and/or an increase in ion energy of ionized species which strike the substrate surface. An increase in ion density is preferably achieved by placing a device inside the etch chamber above the substrate surface, which device enables an increase in the number of ionized particles striking the substrate surface. An example of such a device is an inductive coil which is used to increase the number of ionized species or to maintain the number of ionized species supplied by another source so that an increased number of ionized species are available to strike the substrate surface.

A second preferred method for increasing the number of ionized species is to feed into the process chamber a microwave-generated plasma produced outside of the chamber. It is also possible to increase the number of ionized species by increasing the RF power to an external inductively coupled coil or to increase the DC power to a capacitively coupled source for ion species generation. However, these latter two techniques are less preferred methods for increasing ion density, since the copper (and

alloy metal(s)) atoms generated during etching affect the performance of an external coil and since capacitively coupled species generation is not very efficient. By ion energy, it is meant the energy of the ion at the time it strikes the substrate surface. A second preferred enhanced physical bombardment technique is increasing (to the limit that the substrate is detrimentally affected) the ion energy. Ion energy may be increased by increasing an offset bias on the substrate which attracts the ionized species toward the substrate. This is typically done by increasing the RF power to a platen on which the substrate sets. The effectiveness of an increase in the bias power is dependent upon the RF frequency and the ratio of the bias grounding area to the surface area of the substrate. Ion energy is further increased by operating the etch process chamber at a lower pressure.

A third enhanced physical bombardment technique is a pulsing of the ion density or the ion energy. One preferred means of pulsing the ion energy is to pulse the power to the device which produces the ion species or which is used to increase or maintain the number of ionized species available to strike the substrate surface. Such pulsing is preferably applied to a device located internally within the process chamber. The pulsing may be of the feed rate of an externally-generated plasma into the process chamber. Less preferably, the pulsing may be applied to an external inductively coupled source for plasma generation or to a capacitively coupled source for plasma generation. An even more preferred means of pulsing the ion energy is by pulsing the power to the offset bias source which is applied to the substrate. Pulsing of the ion energy reduces the possibility that an excited copper ion leaving the copper surface during etching will reattach to the copper surface in an adjacent location. The pressure in the process vessel may also be pulsed as a means of pulsing the ion energy.

The fourth enhanced physical bombardment technique is the use of thermal phoresis. Thermal phoresis occurs when the temperature of the substrate surface is higher than the temperature of the etch chamber surfaces (walls), whereby particles dislodged from the higher temperature substrate surface are attracted toward the colder chamber surfaces.

It is possible to use a combination of physical ion bombardment with a

chemically reactive ion component, so long as the concentration of the chemically reactive ion component is sufficiently low that the etching is carried out in a physical bombardment dominated etch regime. Preferably this combination technique is carried out at temperatures above about 150 °C and at pressures below about 50 mT. Since the additional energy provided by the physical bombardment is added to the formation of volatile chemical reaction-generated compounds, the copper removal rate is not limited solely to the rate of formation of the volatile compounds and the ability of a low process chamber pressure to facilitate removal of such volatile compounds. When physical ion bombardment dominates the etch process, the pressure in the process chamber can be adjusted, to permit increased ion bombardment. An overall synergistic effect occurs, enhancing the copper atom removal rate. The preferred chemically reactive ion species is a halogen-comprising species or compound having a low molecular weight, such as Cl_2 , HCl , BCl_3 , HBr , CHF_3 , CF_4 , SiCl_4 , and combinations thereof. When a chlorine-comprising species is used, the chlorine-comprising components present in the feed gases to the etch chamber should be no greater than 30 volume % of the gases fed into the etch chamber during the patterned copper etch. A passivating agent such as N_2 , NH_3 , and CH_4 may be used in combination with the chemically reactive ion species. The content of copending application Serial No. 08/ 891,410 is hereby incorporated by reference in its entirety.

Application Serial No. 08/ 911,878 describes an alternative copper etching technology which employs HCl and HBr chemistries in a manner which protects copper from corrosion during the etching process. In particular, copper can be pattern etched in the presence of HCl or HBr while providing the desired feature dimension and integrity if the surface of the copper feature being etched is properly protected during etching. To avoid the trapping of reactive species which can act as a corrosive agent interior of the etched copper surface, hydrogen is applied to that surface. Hydrogen is adsorbed on the copper exterior surface and may be absorbed into the exterior surface of the copper, so that it is available to react with species which would otherwise penetrate that exterior surface and react with the copper interior to that surface. Sufficient hydrogen must be

applied to the exterior surface of the etched portion of the copper feature to prevent incident reactive species present due to etching of adjacent feature surfaces from penetrating the previously etched feature exterior surface.

Although any plasma feed gas component comprising hydrogen, which is capable of generating sufficient amounts of hydrogen, may be used, the most preferred embodiment of the invention provides for the use of a component which contains both hydrogen and halogen. Preferred examples are hydrogen chloride (HCl) and/or hydrogen bromide (HBr), which are used as the principal source of the reactive species for etching copper. Dissociation of the HCl and/or HBr provides large amounts of hydrogen for protection of etched copper surfaces, thereby preventing penetration by reactive species adjacent the etched surface. Additional hydrogen gas may be added to the plasma feed gas which comprises the HCl and/or HBr when the reactive species density in the etch process chamber is particularly high. The hydrogen-releasing, halogen-comprising plasma feed gas component may be used as an additive (producing less than 40 % of the plasma-generated reactive species) in combination with other plasma etching species.

When HCl and/or HBr is used as the principal source of reactive species for the copper etching, the HCl or HBr accounts for at least 40 %, and more preferably at least 50 %, of the reactive species generated by the plasma. Other reactive species may be used for purposes of feature surface passivation during etching or for purposes of feature surface protection after completion or near the completion of feature surface etching. The species added for surface passivation or surface protection during etching of the copper feature preferably make up 30 % or less, or more preferably make up 10 % or less of the plasma-generated reactive species. By way of example, additional gases which may be added to the plasma feed gas include CH_4 , CH_3F , BCl_3 , N_2 , NH_3 , SiCl_4 , CCl_4 , and CHF_3 . Plasma feed gases may include additional inert (non-reactive with copper) gases such as argon, helium, or xenon, to enhance the ionization, or dissociation, or to dilute the reactive species. The critical feature is the availability of hydrogen at the feature surface during the etching process. The content of U.S. Application Serial No. 08/911,878 is hereby incorporated by reference in its entirety.

The above described preferred embodiments are not intended to limit the scope of the present invention, as one skilled in the art can, in view of the present disclosure expand such embodiments to correspond with the subject matter of the invention claimed below.

CLAIMS

I claim:

1. A method for patterning semiconductor device features comprising the steps of:
 - (a) transferring a pattern from a patterned photoresist layer through a layer of high-temperature inorganic masking material;
 - (b) transferring the pattern from a multi-layered structure remaining after step (a) through an underlying layer of a high-temperature organic-based masking material; and
 - (c) removing any photoresist material which remains after step (b).
2. The method of Claim 1, including an additional step:
 - (d) transferring the pattern from the multi-layered structure present after step (c) through at least one feature layer underlying said high-temperature organic-based masking material.
3. The method of Claim 2, including an additional step:
 - (e) removing residual high-temperature organic-based masking layer material from a surface of said feature layer.
4. The method of Claim 3, including an additional step:
 - (f) applying a planarizing layer of an organic-based material having a dielectric constant which is advantageous for purposes of increasing the gate speed of a transistor.
5. The method of Claim 1, including an additional step following step (c), said step comprising:
 - (c-2) removing any portion of said high-temperature inorganic masking material which remains after step (c).

6. The method of Claim 1, wherein said step (b) transfer through said high-temperature organic-based masking material is achieved using an anisotropic plasma etch.
7. The method of Claim 1, wherein said step (c) removal of photoresist is achieved using an oxygen-based plasma in a manner which produces anisotropic etching.
8. The method of Claim 2, wherein said step (d) pattern transfer is achieved in a manner which produces anisotropic etching.
9. The method of Claim 2, wherein at least one feature layer comprises copper.
10. The method of Claim 9, wherein said copper is etched using enhanced physical bombardment.
11. The method of Claim 9, wherein said copper is etched using a combination of enhanced physical bombardment with a chemically reactive ion component.
12. The method of Claim 9, wherein said copper is etched using a chemistry selected from the group consisting of HCl chemistry, HBr chemistry, or a combination thereof.
13. The method of Claim 8, wherein the thickness of said high-temperature inorganic masking material is designed so that this material is consumed during the step (d) pattern transfer.
14. The method of Claim 3, wherein said high-temperature organic-based masking layer material is removed in a manner which produces anisotropic etching.
15. The method of Claim 3, wherein said high-temperature organic-based masking layer material is removed using a combination of enhanced physical bombardment with a

chemically reactive ion component.

16. The method of Claim 3, wherein said high-temperature organic-based masking layer material is removed using a chemistry selected from the group consisting of HCl chemistry, HBr chemistry, or a combination thereof.

17. The method of Claim 3, wherein said high-temperature organic-based masking layer material is removed using a wet stripping technique.

18. The method of Claim 17, wherein said wet stripping technique passivates at least one surface of said feature layer.

19. The method of Claim 1, including an additional step prior to step (a), wherein said high-temperature organic-based masking layer is deposited using a plasma-based technique.

20. The method of Claim 1, including an additional step (x) prior to step (a), wherein said high-temperature organic-based masking layer is deposited using a CVD technique.

21. A method for patterning semiconductor device features comprising the steps of:

(a) developing an imaged layer of high-temperature imageable material into a pattern using a plasma etching technique, to produce a patterned mask which can be used to transfer a desired pattern through underlying layers; and

(b) transferring the pattern formed in step a) through the underlying layer of high-temperature organic-based masking material.

22. The method of Claim 21, including an additional step:

(c) transferring the pattern from the multi-layered structure present after step (b) through at least one feature layer underlying said high-temperature organic-based

masking material.

23. The method of Claim 22, including an additional step:

(d) removing residual high-temperature organic-based masking layer material from a surface of said feature layer.

24. The method of Claim 23, including an additional step:

(e) applying a planarizing layer of an organic-based material having a dielectric constant which is advantageous for purposes of increasing the gate speed of a transistor.

25. The method of Claim 21, wherein said step (b) transfer through said high-temperature organic-based masking material is achieved using an anisotropic plasma etch.

26. The method of Claim 23, wherein said step (d) masking layer material removal is achieved in a manner which produces anisotropic etching.

27. The method of Claim 23, wherein at least one feature layer comprises copper.

28. The method of Claim 27, wherein said copper is etched using enhanced physical bombardment.

29. The method of Claim 27, wherein said copper is etched using a combination of enhanced physical bombardment with a chemically reactive ion component.

30. The method of Claim 27, wherein said copper is etched using a chemistry selected from the group consisting of HCl chemistry, HBr chemistry, or a combination thereof.

31. The method of Claim 23, wherein the thickness of said high-temperature inorganic

masking material is designed so that this material is consumed during the step (c) pattern transfer.

32. The method of Claim 23, wherein said high-temperature organic-based masking layer material is removed in a manner which produces anisotropic etching.

33. The method of Claim 23, wherein said high-temperature organic-based masking layer material is removed using a combination of enhanced physical bombardment with a chemically reactive ion component.

34. The method of Claim 23, wherein said high-temperature organic-based masking layer material is removed using a chemistry selected from the group consisting of HCl chemistry, HBr chemistry, or a combination thereof.

35. The method of Claim 23, wherein said high-temperature organic-based masking layer material is removed using a wet stripping technique.

36. The method of Claim 35, wherein said wet stripping technique passivates at least one surface of said feature layer.

37. The method of Claim 21, including an additional step (x) prior to step (a), wherein said high-temperature imageable material is material is deposited using a silane-based or TEOS-based chemistry.

38. The method of Claim 37, including an additional step (y) prior to step (x), wherein said high-temperature organic-based masking layer is deposited using a plasma-based technique.

39. The method of Claim 37, including an additional step (z) prior to step (x), wherein

said high-temperature organic-based masking layer is deposited using a CVD technique.

40. A mask stack for etching a semiconductor feature, said mask stack comprising:

- (a) a layer of a low-temperature imageable material;
- (b) a layer of a high-temperature inorganic material underlying said low-temperature imageable material; and
- (c) a layer of a high-temperature organic-based material underlying said high-temperature inorganic material.

41. The mask stack of Claim 40, wherein said high-temperature organic-based layer is comprised of an α -C or an α -FC material.

42. The mask etch stack of Claim 41, wherein said α -C or an α -FC layer is formed using CVD techniques.

43. A mask stack for etching a semiconductor feature, said mask stack comprising:

- (a) a layer of a high-temperature imageable material; and
- (b) a layer of a high-temperature organic-based material underlying said high-temperature imageable material.

44. The mask stack of Claim 43, wherein said high-temperature imageable layer is formed from a silane-based starting material or using TEOS-based chemistry.

45. The mask stack of Claim 44, wherein said high-temperature organic-based layer is comprised of an α -C or an α -FC material.

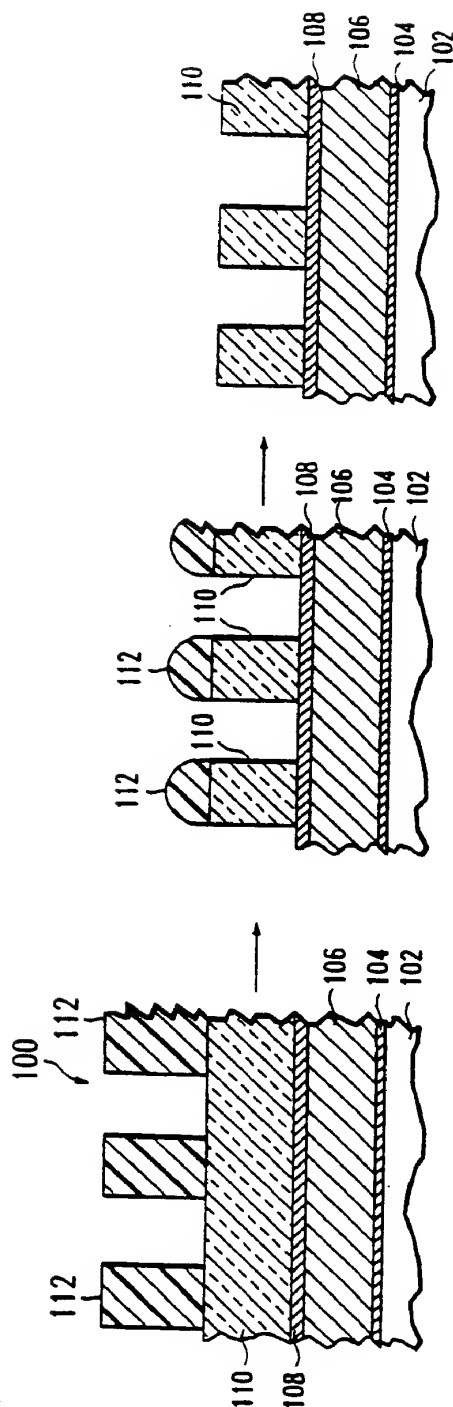


FIG. 1C (PRIOR ART)

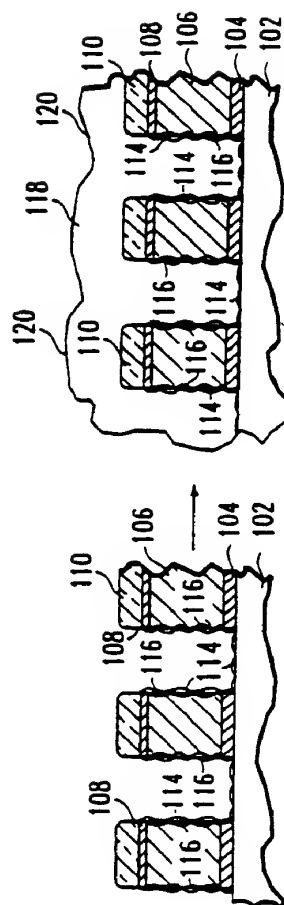


FIG. 1D (PRIOR ART)

FIG. 1E (PRIOR ART)

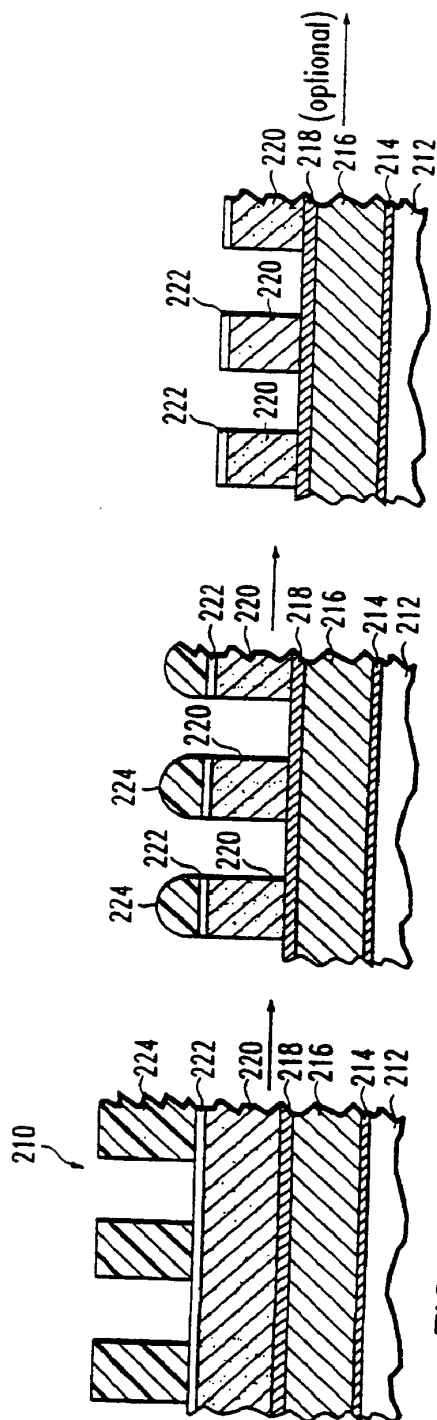


FIG. 2A

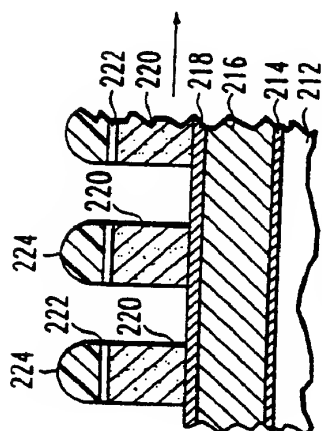


FIG. 2B

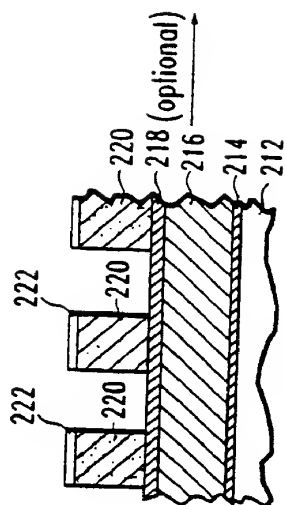


FIG. 2C

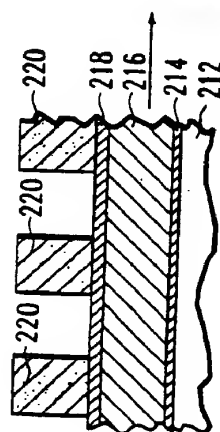


FIG. 2D

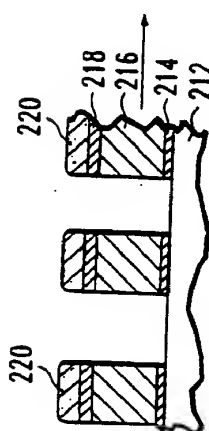


FIG. 2E

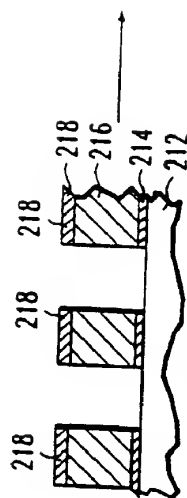


FIG. 2F

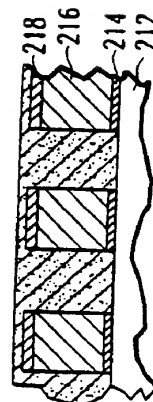


FIG. 2G

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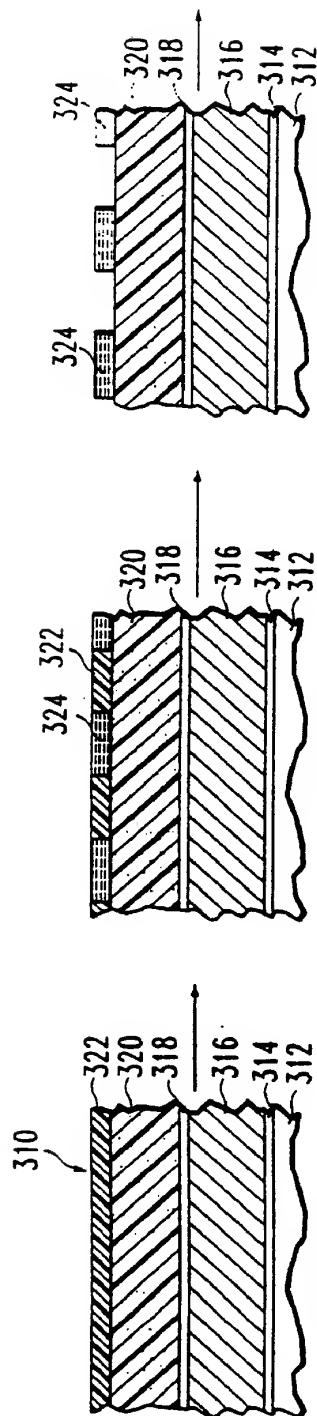


FIG. 3C

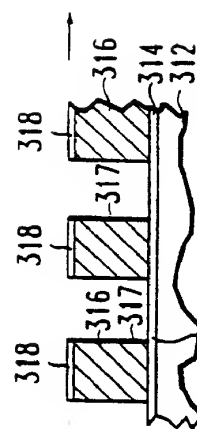


FIG. 3B

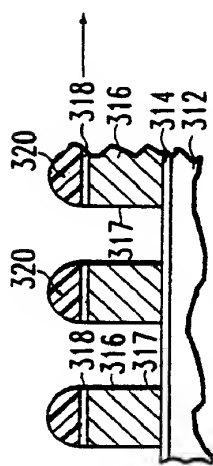


FIG. 3F

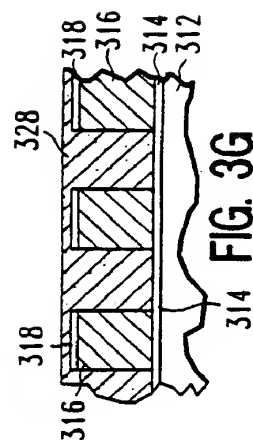


FIG. 3E

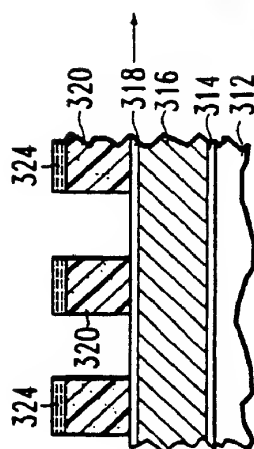


FIG. 3D

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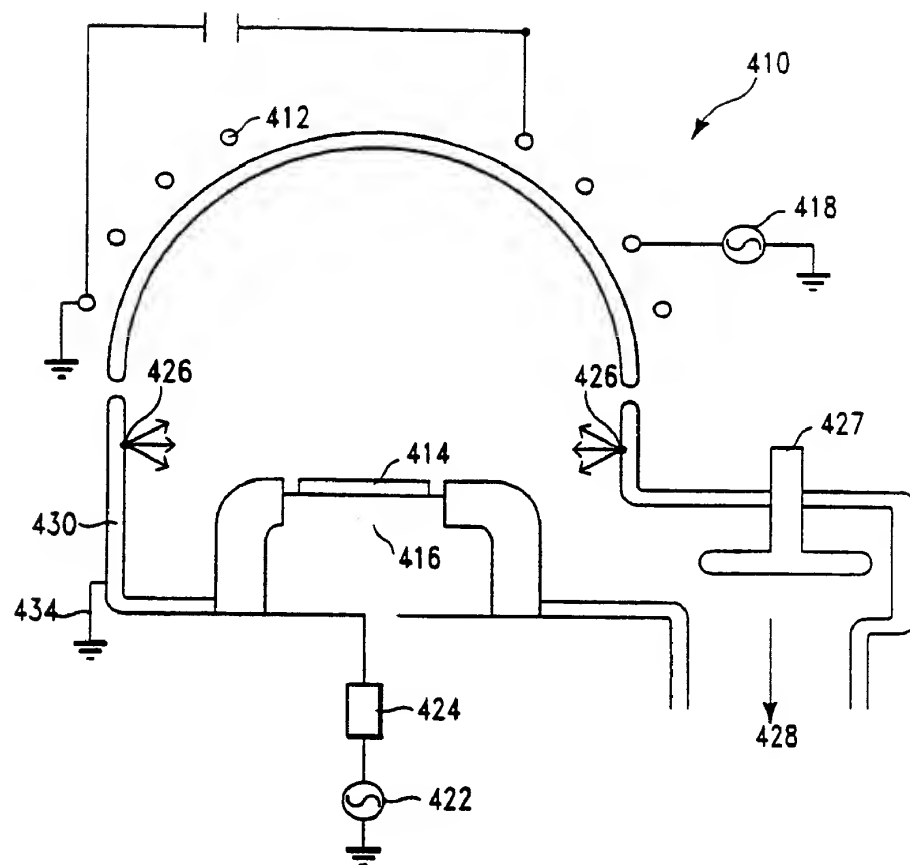


FIG. 4 (PRIOR ART)

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 98/25699

A. CLASSIFICATION OF SUBJECT MATTER IPC 6 H01L21/033 H01L21/3213				
According to International Patent Classification (IPC) or to both national classification and IPC				
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC 6 H01L				
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched				
Electronic data bases consulted during the international search (name of data base and, where practical, search terms used)				
C. DOCUMENTS CONSIDERED TO BE RELEVANT				
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.		
X	EP 0 531 232 A (EASTMAN KODAK CO) 10 March 1993 see column 3, line 30 - column 4, line 43; figure 1	1-3, 6-8, 14, 15, 19, 20		
X	US 4 863 557 A (KOKAKU YUICHI ET AL) 5 September 1989 see column 3, line 17 - line 58; figure 3 --- -/--	43-45		
<input checked="" type="checkbox"/> Further documents are listed in the continuation of box C.				
<input checked="" type="checkbox"/> Patent family members are listed in annex.				
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Date of the actual completion of the international search 1 April 1999		Date of mailing of the international search report 12/04/1999		
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Int. l. Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>US 5 445 710 A (HORI MASARU ET AL) 29 August 1995</p> <p>see column 13, line 1 - line 19 see column 13, line 55 - column 14, line 35 see column 17, line 30 - column 18, line 2; figures 4,9</p> <p>---</p>	<p>1-3,5,6, 9-12, 14-16, 21-23, 25-30</p>
A	<p>US 5 578 166 A (HIROTA TAKATOSHI) 26 November 1996 see column 3, line 47 - column 4, line 65; figure 1</p> <p>---</p>	<p>1-4, 21-24</p>
A	<p>JOUBERT O ET AL: "Application of Plasma Polymerized Methylsilane in an all dry resist process for 193 and 248 nm Lithography" MICROELECTRONIC ENGINEERING, vol. 30, no. 1, January 1996, page 275-278 XP004003081 see figure 2</p> <p>-----</p>	<p>21,37, 38,40,43</p>

INTERNATIONAL SEARCH REPORT

Information on patent family members

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